

PCT

INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

Applicant's or agent's file reference P. IMEC.96/W0	FOR FURTHER ACTION see Notification of Transmittal of International Search Report (Form PCT/ISA/220) as well as, where applicable, item 5 below.	
International application No. PCT/BE 98/ 00139	International filing date (day/month/year) 22/09/1998	(Earliest) Priority Date (day/month/year) 22/09/1997
Applicant INTERUNIVERSITAIR MICRO-ELEKTRONICA CENTRUM et al.		

This International Search Report has been prepared by this International Searching Authority and is transmitted to the applicant according to Article 18. A copy is being transmitted to the International Bureau.

This International Search Report consists of a total of 4 sheets.

☒ It is also accompanied by a copy of each prior art document cited in this report.

1. ☐ Certain claims were found unsearchable (see Box I).
2. ☐ Unity of invention is lacking (see Box II).
3. ☐ The international application contains disclosure of a **nucleotide and/or amino acid sequence listing** and the international search was carried out on the basis of the sequence listing
 - ☐ filed with the international application.
 - ☐ furnished by the applicant separately from the international application,
 - ☐ but not accompanied by a statement to the effect that it did not include matter going beyond the disclosure in the international application as filed.
 - ☐ Transcribed by this Authority
4. With regard to the **title**, ☒ the text is approved as submitted by the applicant
 - ☐ the text has been established by this Authority to read as follows:
5. With regard to the **abstract**,
 - ☐ the text is approved as submitted by the applicant
 - ☒ the text has been established, according to Rule 38.2(b), by this Authority as it appears in Box III. The applicant may, within one month from the date of mailing of this International Search Report, submit comments to this Authority.
6. The figure of the **drawings** to be published with the abstract is:
 - Figure No. 1 ☒ as suggested by the applicant. ☐ None of the figures.
 - ☐ because the applicant failed to suggest a figure.
 - ☐ because this figure better characterizes the invention.

INTERNATIONAL SEARCH REPORT

International application No.

PCT/BE 98/00139

Box III TEXT OF THE ABSTRACT (Continuation of item 5 of the first sheet)

The abstract has been modified as follows:

Delete the last part beginning with the sentence:
"According to another preferred embodiment..."

A. CLASSIFICATION OF SUBJECT MATTER

IPC 6 H04N3/15 H04N5/217

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 6 H04N

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 0 773 669 A (IMEC INTER UNI MICRO ELECTR) 14 May 1997 see column 4, line 15 - line 39 see column 7, line 19 - line 30 ---	5,9
X	US 5 321 528 A (NAKAMURA KENICHI) 14 June 1994 see column 3, line 56 - column 4, line 53; claims 1-4 ---	5,9
X	MARTIN W J ET AL: "DYNAMIC OFFSET NULL" IBM TECHNICAL DISCLOSURE BULLETIN, vol. 23, no. 9, February 1981, page 4195/4196 XP002052268 see the whole document --- -/--	5,9



Further documents are listed in the continuation of box C.



Patent family members are listed in annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search

13 November 1998

Date of mailing of the international search report

18/12/1998

Name and mailing address of the ISA

European Patent Office, P.B. 5818 Patentlaan 2
NL - 2280 HV Rijswijk
Tel. (+31-70) 340-2040, Tx. 31 651 epo nl,
Fax: (+31-70) 340-3016

Authorized officer

Bequet, T

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 0 260 954 A (CANON KK) 23 March 1988 see column 13, line 62 - column 14, line 17; figure 10	3-5,7
A	----	1,6
A	EP 0 481 373 A (SONY CORP) 22 April 1992 see column 4, line 31 - line 52; figure 1 -----	1,6

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No

PCT/BE 98/00139

Patent document cited in search report		Publication date	Patent family member(s)	Publication date
EP 0773669	A	14-05-1997	NONE	
US 5321528	A	14-06-1994	JP 4207564 A CA 2056667 A DE 69124347 D DE 69124347 T EP 0488674 A	29-07-1992 31-05-1992 06-03-1997 28-05-1997 03-06-1992
EP 0260954	A	23-03-1988	JP 2505768 B JP 63076583 A JP 8004127 B JP 63086471 A JP 2510543 B JP 63152280 A JP 8015321 B JP 63152281 A DE 3752018 D DE 3752018 T EP 0741493 A US 4914519 A US 5737016 A US 5331421 A US 5771070 A US 5311320 A	12-06-1996 06-04-1988 17-01-1996 16-04-1988 26-06-1996 24-06-1988 14-02-1996 24-06-1988 20-03-1997 12-06-1997 06-11-1996 03-04-1990 07-04-1998 19-07-1994 23-06-1998 10-05-1994
EP 0481373	A	22-04-1992	JP 4154282 A DE 69116975 D DE 69116975 T US 5187583 A	27-05-1992 21-03-1996 12-09-1996 16-02-1993

From the INTERNATIONAL SEARCHING AUTHORITY

PCTNOTIFICATION OF TRANSMITTAL OF
THE INTERNATIONAL SEARCH REPORT
OR THE DECLARATION

(PCT Rule 44.1)

To:

OFFICE VAN MALDEREN
Place Reine Fabiola 6/1
1083 Bruxelles
BELGIUM

21.12.1998

OFFICE VAN MALDEREN

Date of mailing
(day/month/year)

18/12/1998

Applicant's or agent's file reference

P. IMEC.96/W0

FOR FURTHER ACTION

See paragraphs 1 and 4 below

International application No.

PCT/BE 98/00139

International filing date
(day/month/year)

22/09/1998

Applicant

INTERUNIVERSITAIR MICRO-ELEKTRONICA CENTRUM et al.

- 1.
- ☒
- The applicant is hereby notified that the International Search Report has been established and is transmitted herewith.

Filing of amendments and statement under Article 19

The applicant is entitled, if he so wishes, to amend the claims of the International Application (see Rule 46):

When? The time limit for filing such amendments is normally 2 months from the date of transmittal of the International Search Report; however, for more details, see the notes on the accompanying sheet.**Where?** Directly to the International Bureau of WIPO
34, chemin des Colombettes
1211 Geneva 20, Switzerland
Facsimile No.: (41-22) 740.14.35

For more detailed instructions, see the notes on the accompanying sheet.

- 2.
- ☐
- The applicant is hereby notified that no International Search Report will be established and that the declaration under Article 17(2)(a) to that effect is transmitted herewith.

- 3.
- ☐
- With regard to the protest against payment of (an) additional fee(s) under Rule 40.2, the applicant is notified that:

☐ the protest together with the decision thereon has been transmitted to the International Bureau together with the applicant's request to forward the texts of both the protest and the decision thereon to the designated Offices.☐ no decision has been made yet on the protest; the applicant will be notified as soon as a decision is made.

- 4.
- Further action(s):**
- The applicant is reminded of the following:

Shortly after 18 months from the priority date, the international application will be published by the International Bureau. If the applicant wishes to avoid or postpone publication, a notice of withdrawal of the international application, or of the priority claim, must reach the International Bureau as provided in Rules 90bis.1 and 90bis.3, respectively, before the completion of the technical preparations for international publication.

Within 19 months from the priority date, a demand for international preliminary examination must be filed if the applicant wishes to postpone the entry into the national phase until 30 months from the priority date (in some Offices even later).

Within 20 months from the priority date, the applicant must perform the prescribed acts for entry into the national phase before all designated Offices which have not been elected in the demand or in a later election within 19 months from the priority date or could not be elected because they are not bound by Chapter II.

Name and mailing address of the International Searching Authority

European Patent Office, P.B. 5818 Patentlaan 2
NL-2280 HV Rijswijk
Tel. (+31-70) 340-2040. Tx. 31 651 epo nl.
Fax: (+31-70) 340-3016

Authorized officer

Patricia Klingens-Herklots

PCT

INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

Applicant's or agent's file reference P. IMEC. 96/WO	FOR FURTHER ACTION see Notification of Transmittal of International Search Report (Form PCT/ISA/220) as well as, where applicable, item 5 below.	
International application No. PCT/BE 98/ 00139	International filing date (day/month/year) 22/09/1998	(Earliest) Priority Date (day/month/year) 22/09/1997
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☐ furnished by the applicant separately from the international application.

☐ but not accompanied by a statement to the effect that it did not include matter going beyond the disclosure in the international application as filed.

☐ Transcribed by this Authority

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Figure No. 1 ☒ as suggested by the applicant.

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☐ because the applicant failed to suggest a figure.

☐ because this figure better characterizes the invention.

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According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 6 H04N

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Further documents are listed in the continuation of box C.



Patent family members are listed in annex.

° Special categories of cited documents:

- "A" document defining the general state of the art which is not considered to be of particular relevance
- "E" earlier document but published on or after the international filing date
- "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
- "O" document referring to an oral disclosure, use, exhibition or other means
- "P" document published prior to the international filing date but later than the priority date claimed

- "T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
- "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
- "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.
- "&" document member of the same patent family

Date of the actual completion of the international search

13 November 1998

Date of mailing of the international search report

18/12/1998

Name and mailing address of the ISA

European Patent Office, P.B. 5818 Patentlaan 2
NL - 2280 HV Rijswijk
Tel. (+31-70) 340-2040, Tx. 31 651 epo nl,
Fax: (+31-70) 340-3016

Authorized officer

Bequet, T

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No

PCT/BE 98/00139

Patent document cited in search report		Publication date	Patent family member(s)	Publication date
EP 0773669	A	14-05-1997	NONE	
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EP 0481373	A	22-04-1992	JP 4154282 A DE 69116975 D DE 69116975 T US 5187583 A	27-05-1992 21-03-1996 12-09-1996 16-02-1993

PATENT COOPERATION TREATY

PCT

NOTIFICATION OF THE RECORDING OF A CHANGE

(PCT Rule 92bis.1 and
Administrative Instructions, Section 422)

From the INTERNATIONAL BUREAU

To:

VAN MALDEREN, Joëlle
Office Van Malderen
Place Reine Fabiola 6/1
B-1083 Brussels
BELGIQUE

REQU

18 - 1 - 1999

OFFICE VAN MALDEREN

Date of mailing (day/month/year) 11 January 1999 (11.01.99)	
Applicant's or agent's file reference P.IMEC.96/WO	IMPORTANT NOTIFICATION
International application No. PCT/BE98/00139	International filing date (day/month/year) 22 September 1998 (22.09.98)

1. The following indications appeared on record concerning: <input checked="" type="checkbox"/> the applicant <input checked="" type="checkbox"/> the inventor <input type="checkbox"/> the agent <input type="checkbox"/> the common representative		
Name and Address <div style="border: 1px solid black; height: 100px; width: 100%;"></div>	State of Nationality <div style="border: 1px solid black; height: 100px; width: 100%;"></div>	State of Residence <div style="border: 1px solid black; height: 100px; width: 100%;"></div>
2. The International Bureau hereby notifies the applicant that the following change has been recorded concerning: <input checked="" type="checkbox"/> the person <input checked="" type="checkbox"/> the name <input checked="" type="checkbox"/> the address <input type="checkbox"/> the nationality <input type="checkbox"/> the residence		
Name and Address KAVADIAS, Spyros Predikherinnenstraat 6 B-3000 Leuven Belgium	State of Nationality GR	State of Residence BE
3. Further observations, if necessary: The above-identified person shall be added to the records as applicant/inventor for the United States of America only.		
4. A copy of this notification has been sent to: <div style="display: flex; justify-content: space-between;"> <div style="width: 45%;"> <input checked="" type="checkbox"/> the receiving Office <input checked="" type="checkbox"/> the International Searching Authority <input type="checkbox"/> the International Preliminary Examining Authority </div> <div style="width: 45%;"> <input type="checkbox"/> the designated Offices concerned <input type="checkbox"/> the elected Offices concerned <input type="checkbox"/> other: </div> </div>		

The International Bureau of WIPO 34, chemin des Colombettes 1211 Geneva 20, Switzerland Facsimile No.: (41-22) 740.14.35	Authorized officer <div style="text-align: center;"> Beate Giffo-Schmitt </div> Telephone No.: (41-22) 338.83.38
--	---

PCT

REQUEST

The undersigned requests that the present international application be processed according to the Patent Cooperation Treaty.

For receiving Office use only

International Application No.

International Filing Date

Name of receiving Office and "PCT International Application"

Applicant's or agent's file reference P. IMEC.96/WO
(if desired) (12 characters maximum)

Box No. I TITLE OF INVENTION DEVICES AND METHODS FOR IMPROVING THE IMAGE QUALITY IN AN IMAGE SENSOR

Box No. II APPLICANT

Name and address: (Family name followed by given name; for a legal entity, full official designation. The address must include postal code and name of country. The country of the address indicated in this Box is the applicant's State (that is, country) of residence if no State of residence is indicated below.)

INTERUNIVERSITAIR MICRO-ELEKTRONICA CENTRUM
Vereniging Zonder Winstbejag
Kapeldreef 75
B-3001 HEVERLEE
BELGIUM

☐ This person is also inventor.

Telephone No.

Facsimile No.

Teleprinter No.

State (that is, country) of nationality:
BE

State (that is, country) of residence:
BE

This person is applicant for the purposes of:

☐

all designated States

☒

all designated States except the United States of America

☐

the United States of America only

☐

the States indicated in the Supplemental Box

Box No. III FURTHER APPLICANT(S) AND/OR (FURTHER) INVENTOR(S)

Name and address: (Family name followed by given name; for a legal entity, full official designation. The address must include postal code and name of country. The country of the address indicated in this Box is the applicant's State (that is, country) of residence if no State of residence is indicated below.)

DIERICKX Bart
Cornelis Deherdstraat 8
B-2640 MOTSEL
BELGIUM

This person is:

☐ applicant only

☒ applicant and inventor

☐ inventor only (If this check-box is marked, do not fill in below.)

State (that is, country) of nationality:
BE

State (that is, country) of residence:
BE

This person is applicant for the purposes of:

☐

all designated States

☐

all designated States except the United States of America

☒

the United States of America only

☐

the States indicated in the Supplemental Box

☐ Further applicants and/or (further) inventors are indicated on a continuation sheet.

Box No. IV AGENT OR COMMON REPRESENTATIVE; OR ADDRESS FOR CORRESPONDENCE

The person identified below is hereby/has been appointed to act on behalf of the applicant(s) before the competent International Authorities as:

☒

agent

☐

common representative

Name and address: (Family name followed by given name; for a legal entity, full official designation. The address must include postal code and name of country.)

VAN MALDEREN Joëlle
OFFICE VAN MALDEREN
Place Reine Fabiola 6/1
B-1083 BRUSSELS
BELGIUM

Telephone No.

+32 2 4263810

Facsimile No.

+32 2 4263760

Teleprinter No.

☐ Address for correspondence: Mark this check-box where no agent or common representative is/has been appointed and the space above is used instead to indicate a special address to which correspondence should be sent.

Supplemental Box *If the Supplemental Box is not used, this sheet should not be included in the request.*

1. If, in any of the Boxes, the space is insufficient to furnish all the information: in such case, write "Continuation of Box No. ..." [indicate the number of the Box] and furnish the information in the same manner as required according to the captions of the Box in which the space was insufficient, in particular:
- (i) if more than two persons are involved as applicants and/or inventors and no "continuation sheet" is available: in such case, write "Continuation of Box No. III" and indicate for each additional person the same type of information as required in Box No. III. The country of the address indicated in this Box is the applicant's State (that is, country) of residence if no State of residence is indicated below;
 - (ii) if, in Box No. II or in any of the sub-boxes of Box No. III, the indication "the States indicated in the Supplemental Box" is checked: in such case, write "Continuation of Box No. II" or "Continuation of Box No. III" or "Continuation of Boxes No. II and No. III" (as the case may be), indicate the name of the applicant(s) involved and, next to (each) such name, the State(s) (and/or, where applicable, ARIPO, Eurasian, European or OAPI patent) for the purposes of which the named person is applicant;
 - (iii) if, in Box No. II or in any of the sub-boxes of Box No. III, the inventor or the inventor/applicant is not inventor for the purposes of all designated States or for the purposes of the United States of America: in such case, write "Continuation of Box No. II" or "Continuation of Box No. III" or "Continuation of Boxes No. II and No. III" (as the case may be), indicate the name of the inventor(s) and, next to (each) such name, the State(s) (and/or, where applicable, ARIPO, Eurasian, European or OAPI patent) for the purposes of which the named person is inventor;
 - (iv) if, in addition to the agent(s) indicated in Box No. IV, there are further agents: in such case, write "Continuation of Box No. IV" and indicate for each further agent the same type of information as required in Box No. IV;
 - (v) if, in Box No. V, the name of any State (or OAPI) is accompanied by the indication "patent of addition," or "certificate of addition," or if, in Box No. V, the name of the United States of America is accompanied by an indication "continuation" or "continuation-in-part": in such case, write "Continuation of Box No. V" and the name of each State involved (or OAPI), and after the name of each such State (or OAPI), the number of the parent title or parent application and the date of grant of the parent title or filing of the parent application;
 - (vi) if, in Box No. VI, there are more than three earlier applications whose priority is claimed: in such case, write "Continuation of Box No. VI" and indicate for each additional earlier application the same type of information as required in Box No. VI;
 - (vii) if, in Box No. VI, the earlier application is an ARIPO application: in such case, write "Continuation of Box No. VI", specify the number of the item corresponding to that earlier application and indicate at least one country party to the Paris Convention for the Protection of Industrial Property for which that earlier application was filed.
2. If, with regard to the precautionary designation statement contained in Box No. V, the applicant wishes to exclude any State(s) from the scope of that statement: in such case, write "Designation(s) excluded from precautionary designation statement" and indicate the name or two-letter code of each State so excluded.
3. If the applicant claims, in respect of any designated Office, the benefits of provisions of the national law concerning non-prejudicial disclosures or exceptions to lack of novelty: in such case, write "Statement concerning non-prejudicial disclosures or exceptions to lack of novelty" and furnish that statement below.

BOX IV: OTHER AGENTS

 VAN MALDEREN Michel, VAN MALDEREN Eric

PATENT COOPERATION TREATY

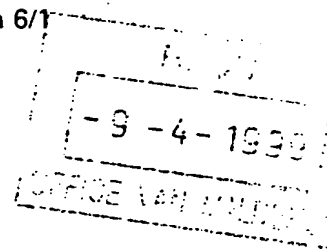
PCT

NOTICE INFORMING THE APPLICANT OF THE
COMMUNICATION OF THE INTERNATIONAL
APPLICATION TO THE DESIGNATED OFFICES

(PCT Rule 47.1(c), first sentence)

From the INTERNATIONAL BUREAU

To:
VAN MALDEREN, Joëlle
Office Van Malderen
Place Reine Fabiola 6/1
B-1083 Brussels
BELGIQUE



Date of mailing (day/month/year) 01 April 1999 (01.04.99)		
Applicant's or agent's file reference P.IMEC.96/WO		IMPORTANT NOTICE
International application No. PCT/BE98/00139	International filing date (day/month/year) 22 September 1998 (22.09.98)	Priority date (day/month/year) 22 September 1997 (22.09.97)
Applicant INTERUNIVERSITAIR MICRO-ELEKTRONICA CENTRUM et al		

1. Notice is hereby given that the International Bureau has communicated, as provided in Article 20, the international application to the following designated Offices on the date indicated above as the date of mailing of this Notice:
AU,BR,CN,EP,IL,JP,KP,KR,US

In accordance with Rule 47.1(c), third sentence, those Offices will accept the present Notice as conclusive evidence that the communication of the international application has duly taken place on the date of mailing indicated above and no copy of the international application is required to be furnished by the applicant to the designated Office(s).

2. The following designated Offices have waived the requirement for such a communication at this time:
AL,AP,BA,BB,BG,CA,CU,CZ,DE,EA,EE,GD,GE,HR,HU,ID,IS,LC,LK,LR,LT,LV,MG,MK,MN,MX,NO,
NZ,OA,PL,RO,SG,SI,SK,SL,TR,TT,UA,UZ,VN,YU

The communication will be made to those Offices only upon their request. Furthermore, those Offices do not require the applicant to furnish a copy of the international application (Rule 49.1(a-bis)).

3. Enclosed with this Notice is a copy of the international application as published by the International Bureau on
01 April 1999 (01.04.99) under No. WO 99/16238

REMINDER REGARDING CHAPTER II (Article 31(2)(a) and Rule 54.2)

If the applicant wishes to postpone entry into the national phase until 30 months (or later in some Offices) from the priority date, a demand for international preliminary examination must be filed with the competent International Preliminary Examining Authority before the expiration of 19 months from the priority date.

It is the applicant's sole responsibility to monitor the 19-month time limit.

Note that only an applicant who is a national or resident of a PCT Contracting State which is bound by Chapter II has the right to file a demand for international preliminary examination.

REMINDER REGARDING ENTRY INTO THE NATIONAL PHASE (Article 22 or 39(1))

If the applicant wishes to proceed with the international application in the national phase, he must, within 20 months or 30 months, or later in some Offices, perform the acts referred to therein before each designated or elected Office.

For further important information on the time limits and acts to be performed for entering the national phase, see the Annex to Form PCT/IB/301 (Notification of Receipt of Record Copy) and Volume II of the PCT Applicant's Guide.

The International Bureau of WIPO 34, chemin des Colombettes 1211 Geneva 20, Switzerland Facsimile No. (41-22) 740.14.35	Authorized officer J. Zahra Telephone No. (41-22) 338.83.38
--	---

© Office Van Malderen
Bxl - 21 September 1998
P.IMEC.96/WO
Stripe-shaped FPN

5

**DEVICES AND METHODS FOR IMPROVING THE IMAGE QUALITY IN AN
IMAGE SENSOR**

10

Field of the invention

The present invention relates to solid state imaging devices being manufactured in a CMOS- or MOS-technology.

15

More particularly, the principal object of the present invention is related to methods and devices which are able to improve the image quality in an image sensor.

20

Another object of the present invention is related to the improvement of the image quality by a method of correcting isolated pixel values present in an image taken by imaging devices.

Background of the invention

25

Solid state image sensors are well known. Virtually all solid-state imaging sensors have as key element a photosensitive element being a photoreceptor, a photo diode, a photo transistor, a CCD gate, or alike. Typically, the signal of such a photosensitive element is

30 a current which is proportional to the amount of electromagnetic radiation (light) falling onto the photosensitive element.

A structure with a photosensitive element included in a circuit having accompanying electronics is

called a pixel. Such pixel can be arranged in an array of pixels so as to build focal plane arrays of rows and columns.

Commonly such solid state image sensors are
5 implemented in a CCD-technology or in a CMOS- or MOS-
technology. Solid state image sensors find a widespread
use in devices such as camera systems. In this application
a matrix of pixels comprising light sensitive elements
constitutes an image sensor, which is mounted in the
10 camera system. The signal of said matrix is measured and
multiplexed to a so-called video-signal.

Of the image sensors implemented in a CMOS-
or MOS-technology, CMOS or MOS image sensors with passive
pixels and CMOS or MOS image sensors with active pixels
15 are distinguished. An active pixel is configured with
means integrated in the pixel to amplify the charge that
is collected on the light sensitive element. Passive
pixels do not have said means and require a charge
sensitive amplifier that is not integrated in the pixel.
20 For this reason, active pixel image sensors are
potentially less sensitive to noise fluctuations than
passive pixels. Due to the additional electronics in the
active pixel, an active pixel image sensor may be equipped
to execute more sophisticated functions, which can be
25 advantageous for the performance of the camera system.
Said functions can include filtering, operation at higher
speed or operation in more extreme illuminations
conditions.

Examples of such imaging sensors are
30 disclosed in EP-A-0739039, in EP-A-0632930 and in
US-A-5608204. The imaging devices based on the pixel
structures as disclosed in these patent applications
however are still subject to deficiencies in the image
quality of the devices.

A problem in these CMOS based imaging devices appears because material imperfections and technology variations have as effect that there is a non-uniformity in the response of the pixels in the array. This effect is
5 caused by a non-uniformity or fixed pattern noise (FPN) or by a photoresponse non-uniformity (PRNU). Correction of the non-uniformity needs some type of calibration, e.g. by multiplying or adding/subtracting the pixel's signals with a correction amount that is pixel-dependent.

10 Several methods to cancel FPN are based on techniques that are often called correlated double sampling or offset compensation. The methods in general are based on the following: the signal of the pixel is subtracted from the signal of the same pixels in a
15 reference state (this reference state is typically the reset or dark state). The difference of both signal is free of pixel-related non-uniformity. However, if the differencing circuit is common for a part of the imager (typically, common for one column), a new non-uniformity
20 will originate due to the non-uniformity of the differencing circuits. In a typical APS imager with common column buffers or column amplifiers, the new fixed pattern noise is column dependent, and is visible in the image as a shade of vertical stripes.

25 A stripe-shaped FPN is much more annoying than a pure statistical FPN. It is seen in experiments that a true random FPN of 5% RMS is barely visible to the human eye, whereas a stripe-shaped FPN remains visible even when the amplitude is below 1% RMS. The reason is
30 that the human eye has a kind of built-in spatial filter that recognises larger structures even when they have low contrast.

Even if in the case that we have no fixed pattern noise, the photoresponse non-uniformity can be different from 0.

Another problem arises due to processing
5 imperfections, statistics, etc. This means that typically, a finite number of pixels in a pixel array will be defective (hard faults) or yield a signal that deviates visibly from the "exact" pixel value. Such faults appear as white or black (or grey) points in the image. This
10 class of faults in the sequel is called an isolated pixel value.

A known way to cancel these spots is to store a list of them and of their positions in the image in a memory unit in the device. In an image processing step,
15 the isolated pixel value is then replaced by e.g. the average of the surrounding pixels. This method is viable, but has the disadvantage that it requires a memory. Moreover, it cannot handle isolated pixel values that appear intermittently or only in certain cases. A good
20 example, is a so-called dark current pixel. Such pixels will appear white in a dark environment, but will behave normal in a bright environment.

Other ways to cancel isolated pixels faults have been proposed, e.g. the spatial median filter or
25 other types of Kalman filters can be used to remove such isolated faults. Unfortunately, such filters do also remove useful detail from the image. Consider the image of a star covered sky with an image sensor that has some faulty pixels that appear white. The quoted filters are
30 not able to remove the white point due to faults, and leave the white points that are stars untouched.

Aim of the invention

The present invention aims to suggest a pixel structure and methods to improve the image quality, more in particular the image non-uniformity of in array of pixels by cancellation of the appearance of column-shaped
 5 fixed pattern noise (FPN).

Main characteristics of the present invention

As a first object, the present invention is related to an image sensor comprising an array of rows and columns of pixels, all the pixels of one column of the
 10 array being connected to at least one common pixel output line having at least one memory element and at least a first amplifying element, all these amplifying elements being connected to a common output amplifier.

According to one preferred embodiment, the
 15 image sensor further comprises :

- a second amplifying element on the output of the memory element,
- said common output amplifier having at least a first and a second input terminals,
- 20 - means for switching the pixel's signal on the common output line and the memory element's signal to respectively first and second amplifying elements of one column, and
- means for switching the two output signals of the
 25 amplifying elements of one column to respectively first and second input terminals of said common output amplifier.

Preferably, the switching means comprise at least one cross-bar switch.

30 According to another preferred embodiment, the image sensor further comprises before the amplifying element two parallel circuits being connected through switches to the common pixel output line, at least one

circuit having said memory element. Preferably, both circuit have a memory element.

According to another preferred embodiment, said common pixel output line is being connected through
5 switches to said memory element and said amplifying element, where the offset of the amplifying element is stored on the memory element during a first phase of the read-out, and this offset is subtracted from the signal of the amplifying element during the second phase of the
10 read-out.

The present invention is also related to a method of reading out an array of rows and columns of pixels in an image sensor as described hereabove according to the first embodiment, comprising the steps of:

- 15 - amplifying the output signals of essentially each pixel of one column in the first amplifying element thereby obtaining a set of amplified pixel output signals,
- amplifying the reference signals of essentially each pixel of one column in the second amplifying element,
20 thereby obtaining a set of amplified pixel reference signals,
- consecutively, for essentially each pixel of said column imposing the amplified pixel output signal to a first or a second terminal of said common output amplifier and
25 imposing the amplified pixel reference signal to a second or a first terminal of said common output amplifier, while switching the amplified pixel output signal to respectively said first and said second terminals for essentially each consecutive pixel of said
30 column, said reference signal being imposed to the other terminal of said common output amplifier.

A voltage can be imposed to a node. In this case, it means e.g. that the node is connected to a

voltage source. The voltage source should be higher than the node, i.e. it should have a lower impedance.

According to another preferred embodiment, the present invention is related to a method of reading
 5 out an array of rows and columns of pixels in an image sensor as described hereabove in the second embodiment of the present invention, comprising the steps of :

- sampling the signal in a first phase and storing it in a memory element,
- 10 - sampling the signal in a second phase and possibly storing it in another memory element,
- subtracting said first signal from said second signal in a unique output circuit.

According to another preferred embodiment,
 15 the present invention is related to a method of reading out an array of rows and columns of pixels in an image sensor as described in the third embodiment of the present invention, comprising the steps of :

- during a first phase, calibrating the output of the
 20 amplifying element to a predetermined value,
- storing said value in a memory element during the application of a first signal of said pixel on the line,
- during a second phase, applying a second signal of said pixel on the line in order to have on the output a signal
 25 proportional to the difference between first and second signals.

Another aspect of the present invention is related to a method of replacing an isolated pixel value in the image of an image sensor, being an array of pixels,
 30 and wherein at least one current source is connected to the pixels, the method comprising the step of :

- limiting said isolated pixel value between or to an upper and/or a lower bound that is derived from the

values of pixels in the immediate neighbourhood of the said isolated pixel value.

Preferably, said upper and/or lower bounds are found by extrapolating the immediate neighbourhood
 5 pixel values towards a value that corresponds to the position of said individual pixel in relation to the immediate neighbourhood pixels.

Said upper and/or lower bounds are found by extrapolating the values of a neighbour (V_1N) of the pixel
 10 having said isolated pixel value and of the neighbour thereafter (V_2N), the replacing pixel value being calculated as $V_1N + n \cdot (V_1N - V_2N)$, n being a real number.

The neighbourhood and the neighbourhood thereafter are on the same row of said array. Preferably,
 15 the upper bound is the maximum of a set of values, said set being determined as the pixel values (a, b, c, d, e) of pixels on the same row of said array as said isolated pixel, said upper bound being calculated as

$$c_{max} = F(a, b, c, d), \text{ or } c_{max} = G(E(a, b), E(e, d), E(b), E(d))$$

 20 where F is a non-linear or linear function, G is a non-linear GE or linear function, E is an extrapolating function, wherein $c_{max} = \text{MAX}(2b - a, 2d - e, b, d)$
 together with

$$c_{min} = \text{MIN}(2b - a, 2d - e, b, d)$$

25 with $\text{MAX}()$ yielding the maximum, respectively the minimum of the arguments, the corrected c -value being obtained as

$$c = \text{MIN}(\text{MAX}(c, c_{min}), c_{max}).$$

30 Brief description of the drawings

Figure 1a represents a particular implementation of a column FPN cancellation method and the

corresponding image sensor structure therefor.

Figure 1b represents an embodiment of a cross-bar switch used in the structure represented in Fig. 1a.

Figure 2 describes another particular implementation of a column FPN cancellation method and the corresponding image sensor structure therefor.

Figure 3 describes a particular embodiment of an output block being used in the structure as represented in Fig. 2.

Figure 4 represents the switching diagram for the read-out signal applied to the several switches in the structure as represented in Fig. 2.

Figures 5 represent another particular implementation of a column FPN cancellation method and the corresponding image sensor structure therefor, wherein Fig. 5a represents more particularly one column in an array of pixels being connected to two different structures represented in details in Fig. 5b and 5c during a first phase and a second phase.

Figure 6 represents the specific topology used for the structure represented in Fig. 5b and 5c.

Figure 7 represents the switching diagram for the read-out sequence to the several switches used in the structure represented in Fig. 6.

Figures 8a and 8b represent a method of correcting isolated white pixel values being present in an image composed by an array of pixels.

Brief description of preferred embodiments of the present invention

As a first object of the present invention, a first structure of an APS image sensor is represented in Fig. 1. References (X_{1j}) , (X_{2j}) and (X_{3j}) are three pixels of a column of an image sensor. The pixel's signal on a common output line (l_j) is represented in particular by the column bus "K" in the present case and is fed to the optional buffer amplifier A_j , and/or stored on a memory element (capacitor C + switch S3), and fed to amplifier B_j . By the relative timing of the addressed pixel's reset pulse and the control of the switch S3, one can make that the pixel's signal and its reference level are available on amplifiers A_j , reps. B_j . The fact that the signal passes through the column amplifiers A_j and B_j , is a source of offset non-uniformity, which is column related and causes a vertical stripe-shaped FPN. More specifically, each column will feature an average "OV" offset voltage referred to the average of the other columns.

Switches (S1) and (S2) are crossbar switches. Suppose that they are in the forward direction either in crossed directions. Both switches S1 and S2 operate synchronously. In both cases, the signal on the capacitor C goes to the input of the output amplifier, and the signal on K goes to the + input of the output amplifier. Yet, the "OV" of the column will be positive in the one case and negative in the other case. Since the switches (S1)/(S2) are modulated, e.g. essentially turned direction at each new row ($i = 1, 2, 3$) of the image, the average offset of a column will be zero. For each individual pixel of a column, there will be indeed remain an offset which

is + or - OV but this is a very small feature, and is not recognised by the eye as a stripe.

Another embodiment of the present invention is to suggest a read-out scheme for image sensors that suppresses the effects of non-uniformities caused by variations in pixels as well as variations in the output amplifiers. This read-out scheme can be used in sensors that provide the output signal in terms of a difference. For example, in a sensor with integrating pixels, this difference is the voltage between the output when the pixel is on reset state and the output voltage after integration time.

Namely the method suggests to subtract the signal when a pixel is reset from the signal after the integration time, in order to have a signal which is free from pixel variations. In order to avoid the introduction of the non-uniform column amplifiers effects, the signal of the reset state as well as the signal after integration are sampled and held by the column read-out circuit. Finally, the subtraction is being carried out by a unique subcircuit at the sensor's output (D). This is detailed in Fig. 2.

For every row of pixels the read-out process is, of course, identical. Let us assume that the i^{th} row is selected. When pixels are reset, the switches controlled by the signal Φ_1 , are closed, thus the reset-level output of every pixel on the i^{th} row, namely x_{ij}^r , is stored on the corresponding memory element M_{rj} (which is in the present case a capacitor).

Then, the switches S_{4j} controlled by Φ_1 are opened and pixels start integrating the charge carriers produced by the impinging light. After the lapse of the

integration time, the switches $S5_j$ controlled by $\Phi2$ are closed, thus storing the values of the pixel output to the memory element M_{Sj} (also a capacitor). This value, for the pixel with coordinates ij is denoted as x_{ij}^s .

5 After the sample and hold phase for the two voltages, x_{ij}^r and x_{ij}^s , for the first column and by proceeding from the first column to the last, the appropriate column read-out circuit is connected with the output.

10 When the i^{th} column has been selected, the signal $\Phi3$ drives the switch $S6_j$ to led the signal x_{ij}^r to the output modified according to the action of the column amplifier, so as a signal

$$y_{ij}^s = A_j x_{ij}^s + B_j \quad (1)$$

15 is led to block D (common output amplifier).

The block D is an easily realisable circuit with an output

$$z(n) = [y(n) - y(n-1)] \quad (2)$$

where $y(n)$ denotes the input as instant n .

20 A preferred embodiment of such output block (D) is described in details in Fig. 3. Therefore, the output signal will be free from variations in the characteristics of pixels and the column amplifiers.

$$y_{ij}^r - y_{ij}^s = A_j (x_{ij}^r - x_{ij}^s) \quad (3)$$

25 where A_j is easily reproducible, by example by using source followers as the local final phase of the column circuits (when $A_j = 2$, $B_j = -V_{thj}$).

Fig. 4 shows a switching diagram for the above-mentioned read-out circuit wherein $\Phi3$ is controlling

S4_j, $\Phi 4$ is controlling the switch S5_j and $\Phi 5$ is controlling the switch S6_j.

According to another embodiment of the present invention, an attempt to overcome the problem of offset introduced by the column in a image sensor consisting of pixels is described in Figs. 5 & 6, which can be used with pixels that are read-out twice in every access. For example, in integrating pixels, one read operation is being performed when the pixel is set on the reset phase (first phase) and the second read-out moment is after a certain integration time (second phase), the first phase is defined by a period wherein the read-out signal of the pixel is according a first state while the second phase is defined by a period such as an integration period where the read-out signal of the pixel is in another state.

In the first phase, when pixel output is V_1 , the capacitor C stores a charge :

$$Q = C(V_{ac} - V_{out}) = C(V_{ac} - V_1 + V_{th}) \quad (4)$$

where V_{th} is the threshold voltage of μ .

During second phase, when pixel output is V_2 , the capacitor stores again charge Q which now can be expressed as :

$$Q = C(V_{g\mu} - V_2) \quad (5)$$

where $V_{g\mu}$ is the gate voltage of μ .

From (4) and (5), we obtain :

$$V_{g\mu} = V_2 - V_1 + V_{ac} + V_{th} \quad (6)$$

Therefore :

$$V_{out} = V_2 - V_1 + V_{ac} \quad (7)$$

i.e. the output voltage does not depend on the V_{th} (where variations in the V_{th} cause offsets in the signal V_{out}).

The column amplifier can be implemented by using the topology described in details in Fig. 6.

Switches S7, S8, S9, S10 and S11 are being controlled by signals $\Phi 5$ and $\Phi 6$ (when Φi is high, the
 5 corresponding switches are closed) as represented in Fig. 7.

According to a preferred embodiment represented in Fig. 7, S7, S8 and S9 are controlled by $\Phi 5$ while S10 and S11 are controlled by $\Phi 6$ (when Φi is high,
 10 the corresponding switches are closed). This means that $\Phi 5$ is describing the situation represented in Fig. 5b while $\Phi 6$ is representing the situation represented in Fig. 5c.

According to another aspect, the present invention is able to discriminate between isolated pixel
 15 faults and features in the real image. In the case of an image of a star covered sky, it should be noted that the fact that the image projected through a lens is never perfectly sharp. Even with good lenses, a star image is not projected on a single pixel. Always the point like
 20 source of the start will be smeared out over a central pixel and a few neighbours. In a 1-dimensional cross section, a star image will look like the image in Fig. 8a, while an isolated pixel fault will look like in Fig. 8b.

In the above simple example, the peak in
 25 Fig. 8b should be removed, while the peak in 8a should remain untouched.

The advantage is clear, only device faults are corrected while normal images are left untouched. The operation causes no visible image degradation in faultless
 30 parts of the image.

According to this second aspect of the present invention, a method to remove an isolated whiter or darker pixel from the image is suggested. This method

consists in limiting the value of every individual pixel between an upper and/or a lower bound that is/are derived from the values of pixels in the intermediate neighbourhood of the said pixel.

5 Preferably, the upper and/or lower bounds are found by extrapolation of the neighbourhood pixel values towards the position of the said individual pixel. The upper and/or lower bound are/is a combination of one or several such 1-D or 2-D extrapolations done with different
10 methods, and/or from different sides of the said individual pixel.

 Preferably, extrapolation is the linear extrapolation of a neighbour (N1) of the said individual pixel (IP) and the neighbour thereafter (N2). The
15 extrapolated value is calculated as $2*N1-N2$ or more general: $N1 + n * (N1-N2)$ where the parameter n is a real number, typically between 0 and 3.

 According to another preferred embodiment, the calculation of the upper bounds is performed by
20 extrapolating values from the two sides of said individual pixels. The advantage is that only the pixels data in 1 line of an image are required, which saves memory and operations and allows straightforward implementation as a pipelined filter. Also such a filter is able to correct a
25 vertical line defect.

 In the example of Figs. 8a and 8b, five pixels in a neighbourhood (a 5-pixel "kernel") are taken. The experience is that smaller kernels do not yield good results. Larger kernels may give some improvements
30 compared to the 5-pixel kernel.

CLAIMS

1. An image sensor comprising an array of rows (i) and columns (j) of pixels (X_{ij}), all the pixels of one column of the array being connected to at least one
5 common pixel output line (l_j) having at least one memory element (M_j) and at least a first amplifying element (A_j), all these amplifying elements (A_j) being connected to a common output amplifier (D), characterised in that the sensor further comprises:
- 10 - a second amplifying element (B_j) on the output of the memory element (M_j),
- said common output amplifier (D) having at least two input terminals,
- means (S1) for switching the pixel's signal on the common
15 output line (l_j) and the memory element's signal (M_j) to respectively third and second amplifying elements (A_j and B_j) of one column, and
- means (S2) for switching the two output signals of the
20 respectively first and second input terminals of said common output amplifier (D).
2. An image sensor as recited in claim 1, wherein said switching means comprise at least one cross-bar switch.
- 25 3. An image sensor comprising an array of columns and rows of pixels (X_{ij}), all the pixels of one column of the array being connected to at least one common pixel output line (l_j) having at least one memory element (M_j) and at least one amplifying element (A_j), all these
30 amplifying elements (A_j) being connected to a common output amplifier (D), characterised in that before the

amplifying element (A_j), the common pixel output line (l_j) is divided through switches ($S4_j$ and $S5_j$) in two parallel circuits, at least one circuit having said memory element (M_j).

5 4. An image sensor as recited in claim 3, wherein both circuits have a memory element (M_{sj} and M_{rj}).

5. An image sensor comprising an array of columns and rows of pixels (X_{ij}), all the pixels of one column of the array being connected to at least one common pixel output line (l_j) having at least one memory element (M_j) and at least one amplifying element (A_j), all these amplifying elements (A_j) being connected to a common output amplifier (D), characterised in that said common pixel output line (l_j) is being connected through switches
10 ($S7_j$, $S8_j$, $S9_j$ and $S10_j$, $S11_j$) to a memory element (C_j) and an amplifying element (μ_j), where the offset of the amplifying element is stored on the memory element during a first phase of the read-out, and this offset is subtracted from the signal of the amplifying element
15 during the second phase of the read-out.
20

6. A method of reading out an array of rows and columns of pixels (X_{ij}) of an image sensor according to claim 1, comprising the steps of :

- amplifying the output signals of essentially each pixel of one column in the first amplifying element (A_j)
25 thereby obtaining a set of amplified pixel output signals,
- amplifying the reference signals of essentially each pixel of one column in the second amplifying element (B_j),
30 thereby obtaining a set of amplified pixel reference signals,

- consecutively, for essentially each pixel ($i = 1, 2, 3$) of said column imposing the amplified pixel output signal to a first or a second terminal of said common output amplifier (D) and imposing the amplified pixel reference signal to a second or a first terminal of said common output amplifier (D), while switching the amplified pixel output signal to respectively said first and said second terminals for essentially each consecutive pixel of said column, said reference signal being imposed to the other terminal of said common output amplifier.

7. A method of reading out an array of rows and columns of pixels (X_{ij}) of an image sensor as recited in claim 3, comprising the steps of :

- sampling the signal in a first phase and storing it in a memory element (M_{ij}),
- sampling the signal in a second phase and possibly storing it in another memory element,
- subtracting said first signal from said second signal in a unique output circuit (D).

8. Method as recited in claim 7, wherein said first phase is the reset phase and said second phase is after the integration period.

9. A method of reading out an array of rows and columns of pixels (X_{ij}) of an image sensor as recited in claim 5, comprising the steps of :

- during a first phase, calibrating the output of the amplifying element to a predetermined value,
- storing said value in a memory element during the application of a first signal of said pixel on the line,
- during a second phase, applying a second signal of said pixel on the line in order to have on the output a signal proportional to the difference between first and second

signals.

ABSTRACT

DEVICES AND METHODS FOR IMPROVING THE IMAGE QUALITY IN AN

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IMAGE SENSOR

The present invention is related to an image sensor comprising an array of rows (i) and columns (j) of pixels (X_{ij}), all the pixels of one column of the array
 10 being connected to at least one common pixel output line (l_j) having at least one memory element (M_j) and at least a first amplifying element (A_j), all these amplifying elements (A_j) being connected to a common output amplifier (D).

15 According to one preferred embodiment, said image sensor comprises :

- a second amplifying element (B_j) on the output of the memory element (M_j),
- said common output amplifier (D) having at least two
 20 input terminals,
- means (S1) for switching the pixel's signal on the common output line (l_j) and the memory element's signal (M_j) to respectively third and second amplifying elements (A_j and B_j) of one column, and
- 25 - means (S2) for switching the two output signals of the amplifying elements (A_j , B_j) of one column to respectively first and second input terminals of said common output amplifier (D).

According to another preferred embodiment,
 30 the common pixel output line (l_j) is divided before the

amplifying element (A_j) in two parallel circuits, at least circuit having said memory element (M_j).

According to a third preferred embodiment, said common pixel output line (l_j) is being connected
5 through switches ($S7_j$, $S8_j$, $S9_j$ and $S10_j$, $S11_j$) to a memory element (C_j) and an amplifying element (μ_j), where the offset of the amplifying element is stored on the memory element during a first phase of the read-out, and this offset is subtracted from the signal of the
10 amplifying element during the second phase of the read-out.

(Figure 1)